

■ DESCRIPTION

The 4826 is the N-Channel logic enhancement mode power field effect transistor, is produced using high cell density advanced trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits.

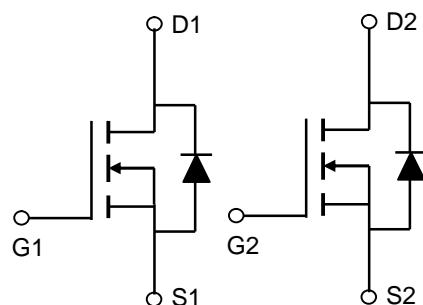
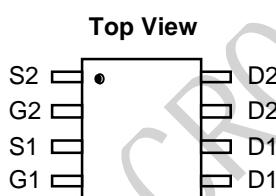
■ FEATURE

- ◆ $60V/8.0A, R_{DS(ON)}=24m\Omega \text{ (typ.)} @ VGS= 10V$
- ◆ $60V/5.0A, R_{DS(ON)}=32m\Omega \text{ (typ.)} @ VGS= 4.5V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOP8 package design

■ APPLICATIONS

- ◆ Power Management
- ◆ Portable Equipment
- ◆ DC/DC Converter
- ◆ Load Switch
- ◆ DSC
- ◆ LCD Display inverter

■ PIN CONFIGURATION



■ PART NUMBER INFORMATION

4826AA-BB C

A= Package Code

S: SOP

BB=Handing Code

TR: Tape&Reel

C=Lead Plating Code

G: Green Product

■ **ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ C$ Unless otherwise noted)

Parameter	Symbol	Maximum		Units
Drain-Source Voltage	V_{DS}	60		V
Gate-Source Voltage	V_{GS}	± 20		V
Continuous Drain Current ^A	I_D	8.0	A	
$T_A=70^\circ C$		5		
Pulsed Drain Current ^B	I_{DM}	40	W	
$T_A=25^\circ C$	P_D	2		
$T_A=70^\circ C$		1.28		
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics					
Parameter	Symbol	Typ	Max	Units	
Maximum Junction-to-Ambient ^A	$t \leq 10s$	$R_{\theta JA}$	50	62.5	°C/W
Maximum Junction-to-Ambient ^A	Steady-State		73	110	°C/W
Maximum Junction-to-Lead ^C	Steady-State	$R_{\theta JL}$	31	40	°C/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

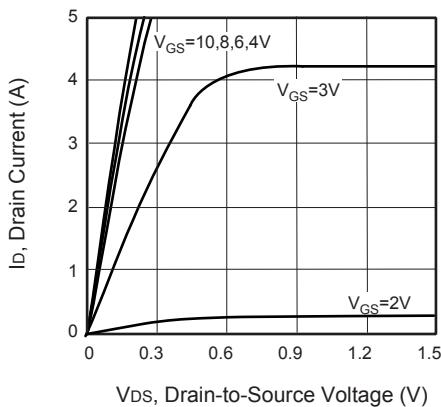
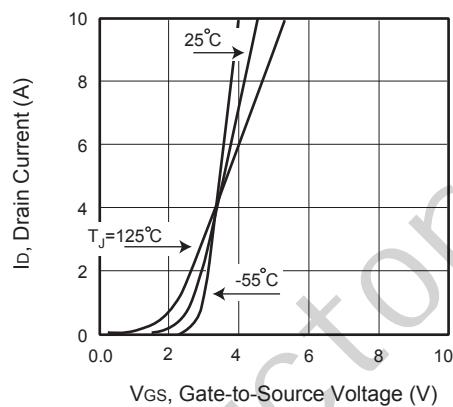
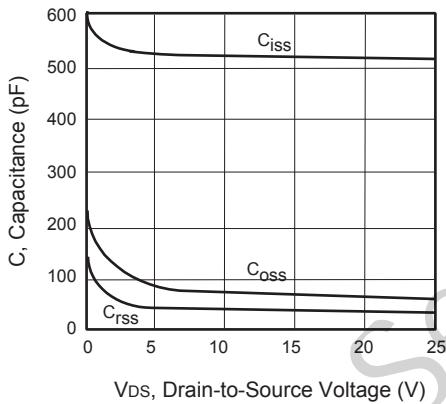
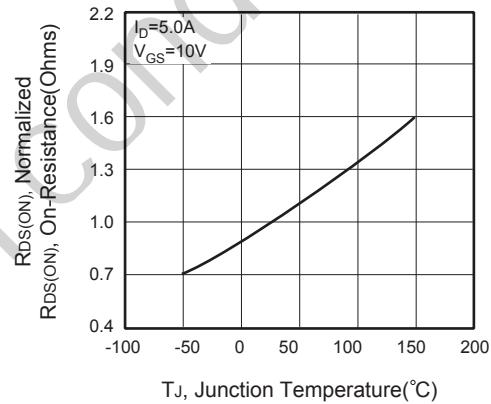
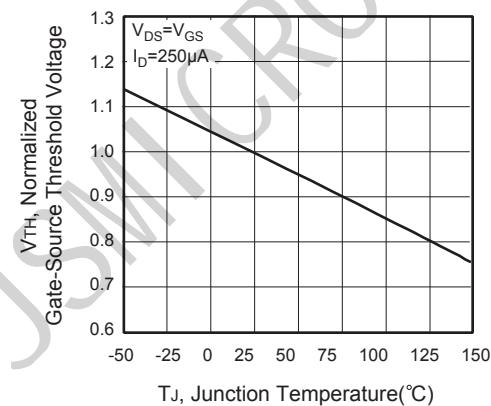
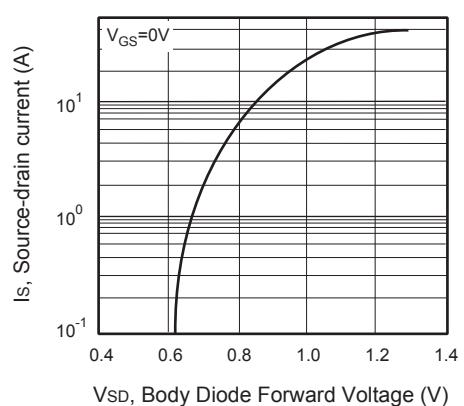
Absolute maximum ratings are stress rating only and functional device operation is not implied

■ **ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ C$ Unless otherwise noted)

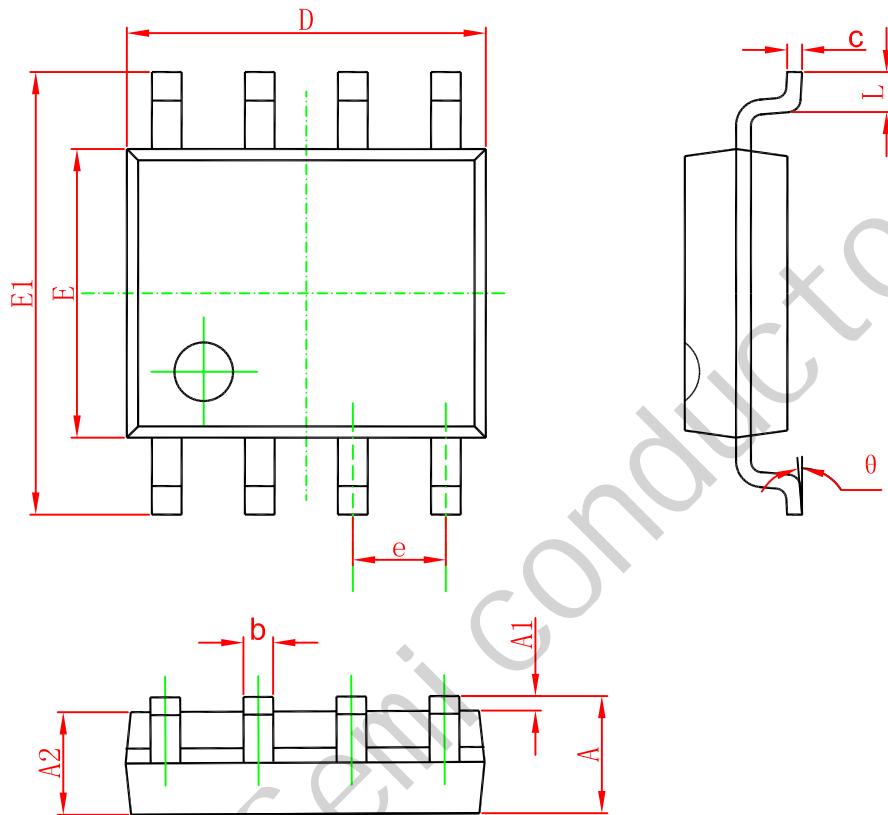
Symbol	Parameter	Condition	Min	Typ	Max	Unit	
Static Parameters							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D= 250\mu A$	60			V	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D= 250\mu A$	1.0	1.8	3.0	V	
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}= 60V, V_{GS}=0$			1	uA	
		$V_{DS}= 60V, V_{GS}=0$ $T_J=55^\circ C$			5		
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}= 10V, I_D= 7.0A$		23	30	mΩ	
		$V_{GS}= 4.5V, I_D= 5.0A$		31	45		
Source-Drain Diode							
V_{SD}	Diode Forward Voltage	$I_S= 1.0A, V_{GS}=0V$		0.8	1.3	V	
Dynamic Parameters							
Q_g	Total Gate Charge	$V_{DS}= 30V$ $V_{GS}= 10V$		15.6	16	nC	
Q_{gs}	Gate-Source Charge			1.3			
Q_{gd}	Gate-Drain Charge			4.5			
C_{iss}	Input Capacitance	$V_{DS}= 5.20V$ $V_{GS}=0V$ $f=1MHz$		520		pF	
C_{oss}	Output Capacitance			105			
C_{rss}	Reverse Transfer Capacitance			60			
$T_{d(on)}$	Turn-On Time	$V_{DS}= 30V$ $I_D= 1A$ $V_{GEN}= 10V$ $R_G=6\Omega$		8	16	nS	
T_r				6	12		
$T_{d(off)}$	Turn-Off Time			25	46		
T_f				4	8		

Note: 1. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

2. Static parameters are based on package level with recommended wire bonding

■ **TYPICAL CHARACTERISTICS (25°C Unless Note)**

Figure 1. Output Characteristics

Figure 2. Transfer Characteristics

Figure 3. Capacitance

Figure 4. On-Resistance Variation with Temperature

Figure 5. Gate Threshold Variation with Temperature

Figure 6. Body Diode Forward Voltage Variation with Source Current

■ SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°